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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Group Art Unit: 1722
Examiner: Mr. Matthew J. Song

In re PATENT APPLICATION of:

Applicant:	Kazutaka SHIBATA	)
Serial No.:	09/830,092	)
Filed:	June 27, 2001	) **APPEAL BRIEF**
For:	SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME	)
Docket No.	AI 264NP	)

March 24, 2006

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Sir:

INTRODUCTION

This is an Appeal to the Board of Patent Appeals and Interferences from the decision, in an Office Action dated December 28, 2005, finally rejecting claims 3, 4, 6, and 26-28. A Notice of Appeal was filed on January 24, 2006. Accordingly, it is respectfully submitted that the present appeal Brief is timely.

A fee of $ 500 is being submitted concurrently. Should this remittance be accidentally missing, however, or should any additional fees be needed (including extension of time fees, since Appellant hereby provisionally petitions for any extensions that may be deemed necessary to avoid abandonment), the Director may charge such fees to our Deposit Account number 18-0002.

FEE ENCLOSED:$ 500
Please charge any further fee to our Deposit Account No. 18-0002

(i) REAL PARTY IN INTEREST

The real party in interest in this appeal is the assignee, Rohm Co., Ltd., having an office in Kyoto, Japan.

(ii) RELATED APPEALS AND INTERFERENCES

To the best of the knowledge and belief of the undersigned attorney, there are no prior or pending appeals, interferences, or judicial proceedings which may be related to, directly affect or be directly affected by, or have a bearing on the Board's decision in the present appeal.

(iii) STATUS OF CLAIMS

Claims 3, 4, 6, 17-20, and 26-29 are pending in this application. Claims 17-20 and 29 have been allowed. Claims 1, 2, 5, 7-16, and 21-25 have been cancelled. Claims 3, 4, 6, and 26-28 stand finally rejected.

(iv) STATUS OF AMENDMENTS

No amendments have been filed in response to the Office Action of December 28, 2005, which will hereafter be called the "Final Rejection."

(v) SUMMARY OF CLAIMED SUBJECT MATTER

The rejected claims are directed to a method for making a semiconductor device. In Figure 3(a) of the application's drawings, electrodes T are connected to pads (not illustrated) on a semiconductor wafer W (page 25, lines 5-22). A resin layer 3 is applied to the top side of the wafer W in Figure 3(b), and covers the top ends of the electrodes T (page 25, line 23 to page 26, line 11). In Figure 3(c), a back side resin layer 4 is applied to the wafer W (page 26, line 12 to page 27, line 7). As a result, thermal expansion or contraction at the front and back sides of the wafer W are approximately equal (page 24, lines 12-16).

In Figure 3(d), part of the resin 3 in the upper ends of the electrodes T are ground away (page 27, lines 8-25), and in Figure 3(e), the back side resin layer 4 is ground away and the wafer itself is thinned (page 28, lines 1-10). The remaining portion of the front-side resin layer 3 reinforces the wafer W not only while the back side is being ground, but also during the front-side grinding (page 28, lines 16-21). In Figure 3(f), a dicing saw 5 is used to cut the wafer into individual semiconductor chips (page 28, lines 11-15) that have a uniform thickness (page 29, lines 19-23).

(vi) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 3, 4, 6, and 26-28 have been rejected for obviousness based on WO 99/09595 by Sekine et al (where U.S. 6,495,914 to Sekine et al is used as a translation) in view of U.S. 6,455,920 to Fukasawa et al and JP 02-031437 by Ichikawa. For the sake of

convenience, U.S. 6,495,914 will hereafter be called simply "Sekine" the Fukasawa et al reference will hereafter be called simply "Fukasawa."

(vii) ARGUMENT

Claim 3 is the sole independent claim in this appeal. With regard to claim 3, the Final Rejection (that is, the Office Action of December 28, 2005) states: "Sekine et al discloses all of the limitations of claim 3, as discussed previously, except a step for forming a back side resin layer on a back side of the semiconductor substrate and removing a back side resin layer through polishing or grinding from the semiconductor substrate." It is not apparent where previous Office Actions have discussed claim 3 with respect to the Sekine reference. At any rate, it is respectfully submitted that there are more differences between Sekine and the invention defined by claim 3 than are acknowledged in the Office Action.

Perhaps the place to begin in Sekine's Figures 4a-4d, since previous Office Actions have drawn attention to features shown in these figures with respect to other claims. The passage at column 6 of Sekine, lines 4-54, basically explains that bare chip devices 47 are deposited in recesses 45 in a base substrate 41, and are then covered by resin 48. The upper portion of the resin is ground away, and wiring and passive components are provided on a layer 50. The back side of the base substrate 41 is ground, leaving structure that includes conductive posts 42 for connection to a motherboard.

The above-noted passage at column 6 of the reference calls Sekine's element 41 a "base substrate." The sentence at column 6, lines 14-16, advises that the markers or recesses 45 "are formed by the press working as in the above embodiment mentioned above and each have a taper." In the embodiments that the reference has previously described, the substrate is clearly metal (see page 4, lines 33-37 and 66-67, and

column 5, lines 46-50) that is etched and then formed by a press to provide the recesses which hold the chips. An ordinarily skilled person would therefore understand that the base substrate 41 in Sekine's Figures 4a-4d is also made of metal.

Claim 3 recites "a step of forming projection electrodes on a surface at a front side of a semiconductor substrate." Sekine's elements 42 are provided at the front side of his substrate 41, but the substrate 41 not a semiconductor substrate. An ordinarily skilled person who wanted to improve Sekine in some way would not tnink of changing his substrate 41 from metal to semiconductor because Sekine's pressing step (to form the recesses 45) would shatter the substrate.

Claim 3 also recites "a step of forming a back side resin layer on a back side of the semiconductor substrate ...". The Final Rejection draws attention to Fukasawa's resin layer 41 on the back surface of a chip (see Figure 23A of the reference, for example), and takes the position that it would have been obvious to modify Sekine with Fukasawa's "resin layer on the bottom of the chip to eliminate damage to the bottom of the semiconductor chip during dicing." But Sekine's substrate 41 is metal, which is typically far less fragile than semiconductor. In addition, Sekine's bare chip devices 47 are already diced. An ordinarily skilled person would therefore have had no incentive to apply Fukasawa's resin layer 41 to the back side of either Sekine's substrate 41 or his bare chip devices 47.

Claim 3 also includes a "back side grinding step of thinning the semiconductor substrate by removing the back side resin layer, through polishing or grinding, from the semiconductor substrate ..., and by further polishing or grinding the back side of the semiconductor substrate from which the back side resin layer has been removed." The Final Rejection acknowledges that neither Sekine nor Fukasawa disclose this, but draws attention to Ichikawa. This reference discloses a semiconductor chip that is bonded face-down onto a circuit board and sealed with resin. The resin on the back side of the chip is then ground away and the chip itself is thinned, thereby reducing the package height.

As was discussed above, an ordinarily skilled person would have had no incentive to modify Sekine by adding Fukasawa's resin layer 41. But even assuming for sake of argument that Fukasawa's resin layer 41 were added somewhere to Sekine's arrangement, there would still be no incentive to modify the result in accordance with Ichikawa. What would be the point of adding a resin layer to the bottom of Sekine's metal substrate 41 and then grinding it away? Furthermore, if a resin layer were added to the bottom of Sekine's bare chip devices 47, it would not be possible to grind the resin layer away. In fact, any grinding that might be done on Sekine's bare chip devices 47 would grind away his bumps 46.

Claim 3 provides that the back side resin layer is formed such that "the surface resin layer and the back side resin layer have substantially the same thickness respectively." The Final Rejection acknowledges that Sekine, Fukasawa, and Ichikawa are silent as to the surface resin and back side resin being substantially the same thickness, but takes the position that it would have been obvious to optimize the thickness of the resin layer by conducting routine experimentation. One problem with this rationale is that, of the many features disclosed in the references that might be optimized in some way, there is no apparent reason why an ordinarily skilled person would have selected the relative thicknesses of front and back resin layers as a feature that needed to be optimized.

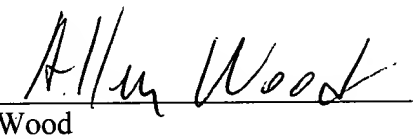
The remaining claims that stand finally rejected depend from claim 3 and recite additional limitations to further define the invention, so they are patentable along with claim 3. Nevertheless, two of the dependent claims will now be briefly addressed.

Dependent claim 4 recites "a cutting out step of cutting out pieces of semiconductor devices by cutting the semiconductor substrate along cutting lines after completing the back side grinding step." Dependent claim 26 also includes a cutting out step. Sekine's base chip devices 47 are already diced, and even if Fukasawa's resin layer were added and ground away, there would still be no reason to further sub-divide the bare chip devices 47.

CONCLUSION

For the foregoing reasons, it is respectfully submitted that the rejected claims are patentable over the references. Accordingly, the Examiner's rejection of these claims should be reversed.

Respectfully submitted,



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(viii) CLAIMS APPENDIX

The claims involved in this appeal are presented below:

Claim 3. A method for manufacturing a semiconductor device, comprising:

a step of forming projection electrodes on a surface at a front side of a semiconductor substrate,

after said step of forming projection electrodes, a step of forming a surface resin layer on the surface of the semiconductor substrate,

a step of forming a back side resin layer on a back side of the semiconductor substrate so that the surface resin layer and the back side resin layer have substantially the same thickness respectively,

a surface grinding step of exposing the projection electrodes from the surface resin layer by polishing or grinding the surface resin layer,

bracing the substrate with the back side resin layer until after the surface grinding step, and

after said surface grinding step, a back side grinding step of thinning the semiconductor substrate by removing the back side resin layer, through polishing or grinding, from the semiconductor substrate provided with the surface resin layer and the back side resin layer, and by further polishing or grinding the back side of the semiconductor substrate from which the back side resin layer has been removed.

Claim 4. A method for manufacturing a semiconductor device as claimed in claim 3, further comprising a cutting out step of cutting out pieces of semiconductor devices by cutting the semiconductor substrate along cutting lines after completing the back side grinding step.

Claim 6. A method for manufacturing a semiconductor device as claimed in claim 3, in which the surface resin layer is formed in such a manner that the projection electrodes are embedded in the surface resin layer.

Claim 26. A method for manufacturing a semiconductor device as claimed in claim 3, further comprising a cutting out step of cutting out pieces of semiconductor devices by cutting the semiconductor substrate along cutting lines after completing the back side grinding step, wherein the surface grinding step includes exposing the projection electrodes from the surface resin layer by polishing or grinding the surface resin layer such that the remaining surface layer has a thickness that is uniform at least within the cutting lines defining the individual pieces cut out of semiconductor devices in the cutting out step.

Claim 27. A method for manufacturing a semiconductor device as claimed in claim 3, wherein said step of forming a surface resin layer includes forming the surface layer with uniform thickness.

Claim 28. A method for manufacturing a semiconductor device as claimed in claim 3, wherein the surface grinding step includes grinding the surface resin layer so that the heights of the plurality of projection electrodes are uniform.

(ix) **EVIDENCE APPENDIX**

No new evidence is being submitted with this Brief.

(x) **RELATED PROCEEDINGS APPENDIX**

In view of section (ii) of this Brief, no copies of decisions are appended.